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Electrical performance of ZnO thin film transistors having different active layer thickness

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In this work, ZnO based thin film transistors (TFTs) were fabricated by sol–gel spin-coating method. We report the changes in ZnO TFTs performance according to the thickness of active layer. As the thickness of channel layer increases, it was observed an increase in the field effect mobility up to 0.34 $cm^2v^{-1}s^{-1}$ for 65 nm and a decrease in the leakage current. But the maximum I_{on}/I_{off} ratio was obtained for 50 nm thickness of ZnO-TFT. This improvement can be attributed to the reduction of channel resistance and enhancement of average grain size.

Keywords: ZnO-TFT, Sol gel spin coating, Field effect mobility, Channel thickness

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1. Introduction

Increasing demand for large area electronic devices and high-performance electronics in recent years has sparked to the development of a new class of electronic materials. Metal oxide semiconductors are promised materials when they are compared with poly-Si and organic semiconductors counterparts because of their high electron mobility and electrical stability. Among metal oxide semiconductors, well-known ZnO semiconductor has unique electrical and optical properties such as wide band gap (3.37 eV), high electron mobility and n-type active layer caused by oxygen vacancies or Zn interstitials [1-2]. ZnO TFTs have great potential applications such as chemical or biosensors [3], photo detectors [4], driver transistors for active-matrix liquid crystal displays [5], photovoltaic solar cells [6] and high electrical performance device.

The electrical performances of TFTs are affected by various factors. These factors can be summarized as the deposition process [7] and crystalline quality of the active layer [8], the doping sources and concentrations [9], the interface properties between active layer and gate dielectric [10], the characteristics of the insulators layer and so on. The thickness of the semiconductors layer also plays a crucial role in the electrical properties of the TFTs [11-12]. This consideration shows that to make characterization and to obtain the maximum performance for TFTs, the modification and the thickness of the active layers must be carefully controlled. So, the optimization of the device fabrication will improve the device performance.

The thickness of active layer directly affects on/off ratio that is one of the essential parameters for TFT. To investigate the effect of variation of the active layer on the leakage current ($I_{ds,off}$), the following equation can be used in case of where the gate voltage is 0 V [12];

$$I_{ds,off} = \frac{\sigma W t}{L} V_{DS} \qquad (1)$$

Where σ is the electrical conductivity, t is the thickness of channel layer, W and L are the width and length of the conduction channel, respectively, and V_{DS} is the source-drain voltage in the equation. According to Eq. (1), if the thickness of ZnO active layer increases, the leakage current (off current) will be increased and on/off rate will be decreased. Therefore the thickness of active layer must be optimized to improve device performance.

A lot of literatures on the synthesis of ZnO TFTs are available, but the thickness of active layer ZnO TFTs, which is deposited by sol–gel spin-coating method, is rarely mentioned.

In this work we fabricated the ZnO TFTs with different thickness active layers varying from 35 nm to 65 nm. We have studied the effect of thickness active layer on the device performance of TFTs. Also, morphological properties of ZnO active layer were investigated.

2. Experimental details

The ZnO precursor was prepared by mixing zinc acetate $[Zn(OAc)_{22}H_2O]$ and monoethanolamine (1:1M ratio) in 2-methoxyethanol at the concentration of 0.05 mol/L. For transparent and homogeneous solution, it was stirred continuously for 2 h at 60 OC. The oxygen plasma was used to remove organic waste from substrate surface. Then, a liquid film was deposited on the 100 nm SiO2 coated Si (highly doped) layer (University wafer, USA) by spin coater with a spin speed of 3000 rpm for 30s in the room temperature. After each coating, ZnO films were placed in an oven for 10 minutes at 300°C. For improvement of some parameters of active layer such as crystallization and grain size, the films were annealed in air at 750 °C for 2h. Obtaining the active layers having different thicknesses was accomplished by repeating the spin-coating process. For 3, 4 and 5 layers, the thicknesses of the obtained ZnO films are about 35 nm, 50 nm and 65 nm, respectively, confirmed by the cross-section SEM image. These films are named Z3, Z4 and Z5 respectively. Following the coating of the ZnO films, aluminum source and drain electrodes having interdigitated-finger geometry were evaporated. The channel width and length of the transistor are 1000 µm and 50 µm, respectively. And then silver paste was used for the gate contact. The schematic structure of ZnO TFT is given in Fig. 1.

The morphological properties of films were investigated by ZEISS Ultraplus model field emission scanning electron microscopy (FE-SEM), respectively. Electrical performance of TFTs was carried out with Keithley 4200 semiconductor characterization system and Signatone Probe Station was used to obtain

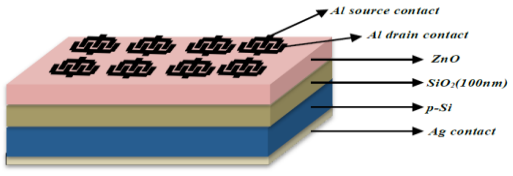


Figure 1. The schematic structure of the ZnO Thin Film Transistor.

3. Results and discussion:

The FE-SEM images give us information about surface morphology, crystallite size and shape for active layer thin films. Fig. 2 shows FE-SEM images of Z3, Z4 and Z5 films taken at 0.5x105 and 4x105 magnifications respectively. It can be seen from Fig.2 that all three films exhibit a smooth, almost uniform and small-grained microstructure. From the illustrated images, formation of wrinkle network and clarity of grain boundaries can be seen as increase in thickness. So, we can say that the average grain size increases with increasing thickness.

To investigate the effect of ZnO film thickness deposited by sol-gel solution-processed on the device performance, TFTs devices were fabricated at different thicknesses.

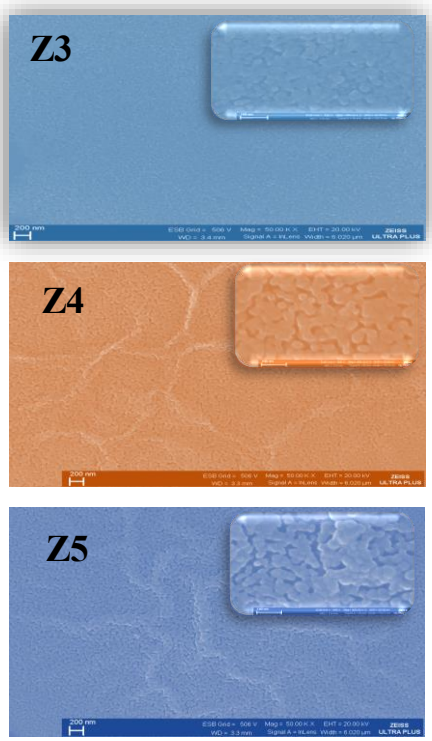


Figure 2. FE-SEM micrographs of the ZnO films deposited at different thickness

Fig. 3 illustrates the output and transfer characteristics of the ZnO TFTs with different thickness. As seen in Fig. 3, the more electron carriers are created with the positive gate biases. It means that the fabricated TFTs exhibit the n-channel behavior due to the n-type electrical conductivity of the ZnO active layer. The conventional transistor model has two region. First, drain current (Ids) is increased linearly at low drain voltages. Second, drain current comes to saturation due to pinch-off of the transistor channel at high drain voltages. Leakage current reaches from a minimum of $1.23x10^{-4}$ A to $3.84\ x10^{-4}$ A for Z3, Z4 and Z5, respectively. The

output characteristic of TFTs shows that the drain current is increased with increasing active layer thickness at off state. Xie et. al. [11] proposed parallel resistance model to explain reduction of active layer resistance. The resistance of active layer near the dielectric layer R_s (surface resistance) and the resistance of active layer away from the interface R_b (bulk resistance) are connected parallel with each other. Therefore, the conductance of channel is defined by the lower one of R_s and R_b. As a result, the drain current of thicker active layer is higher than thinner layer.

The key electrical parameters were calculated to help understanding the performance of ZnO thin film transistors with various thicknesses. As known, the channel mobility (μ_{sat}) and threshold voltage (V_{th}) are very important parameters of TFTs and evaluated by fitting straight lines to the plot of $I_{ds}^{1/2}$ v.s V_{gs} in the saturation region [13]:

$$I_{ds} = \frac{\mu_{sat} C_i W}{2L} \left(V_{gs} - V_{th}\right)^2 \qquad (2)$$

Where, C_i, W, L, V_{gs}, and V_{th} are the capacitance of the insulating layer per unit area, channel width, channel length, gate bias, and threshold voltage, respectively. The obtained all parameters are summarized in Table 1.

Table 1. Electrical properties of ZnO TFTs at different thickness.

One of the most important parameters of the transistor is the field effect mobility, which indicates how easy the charge carriers can drift under the influence of electric field. Also it is an indicator of the performance of semiconductor active layer. The effect of the thickness on the mobility is shown in Table 1.

The increase in mobility is an indicator of the increase in the electrical performance of the device. The saturation mobility (μ_{sat}) for Z3, Z4 and Z5 were found 0.09, 0.24 and 0.34 $cm^2V^{-1}s^{-1}$ respectively. This enhancement at mobility may be attributed to the reduction of channel resistance and decrease in the electron scattering centers due to the increase in average grain size with thickness. [12, 14-15].

Film code	Thickness (nm)	Mobility ($cm^2/V.s$)	V_{th}(V)	I_{on}/I_{off}	Leakage Current (V_G=0V,V_{DS}=40V) (A)
Z3	35	0.09	-30	1.4x10^3	1.23x10^{-4}
Z4	50	0.24	-21	2x10^3	3.18 x10^{-4}
Z5	65	0.34	-35	64	3.84x10^{-4}

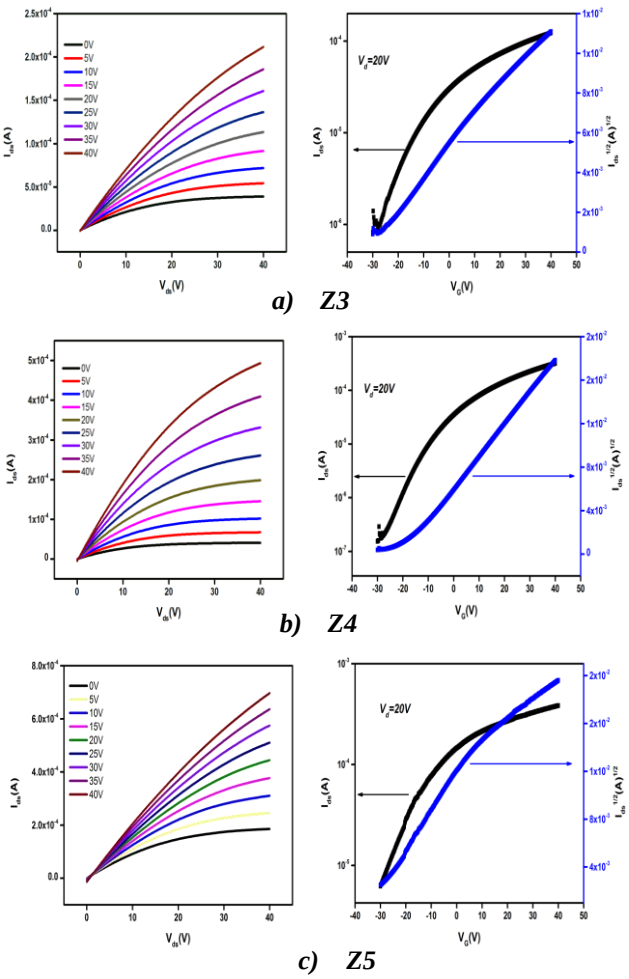


Figure.3 The plots (output characteristics) of drain current versus drain voltage of the ZnO-TFTs and the Transfer characteristics of TFTs

Another important parameter Ion/Ioff ratio for Z3, Z4 and Z5 were found 1.4x10^3, 2x10^3 and 64, respectively. The output characteristics show that Z5 TFT has the highest off-current due to the low channel resistance. As a result, the high off-current decreases I_{on}/I_{off} ratio. The threshold voltage was obtained -30V, -21V and -35V, respectively. All TFTs operate in the depletion mode due to negative threshold voltage.

Conclusions

ZnO TFTs were fabricated by sol–gel spin-coating method with different thickness of the channel layer. FE-SEM images showed that the surface morphology of the film and grain size affected by the film thickness. The electrical characteristics of ZnO TFTs changed significantly with the increase in the channel thickness. In case of the active layer thickness is about 50 nm, better

electrical performance for ZnO TFTs was obtained. The results indicate that an appropriate thickness of channel layer is a key issue for better performance of TFT devices.

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