Journal of Materials and Electronic Devices 6 (2021) 28-32

JOURNAL OF
MATERIALS AND ELECTRONIC DEVICES
FYTRONIX JMED
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Analysis of main electrical characteristics of Al/GO-PTCDA/p-Si structure at room temperature

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We investigated the main electrical characteristics of Al/GO-PTCDA/p-Si structures at room temperature (300 K). The electrical characteristics such as the ideality factor n, the barrier height Φ_{bo}, and the series resistance R_S of the Al/GO-PTCDA/p-Si structure can be determined with one single *I-V* measurement. The current–voltage (*I–V*) characteristics of the Al/GO-PTCDA/p-Si structures were analyzed by the thermionic emission theory. Furthermore, the energy distribution of interface states density (N_{SS}) as a function of energy distribution (E_{SS}- E_V) were determined from the forward bias *I–V* characteristics by taking into account the bias dependence of the effective barrier height. The results show that the values of the main electrical properties are important parameters to determine the properties of Al/GO-PTCDA/*p*-Si structures.

Keywords: *Si, Electrical properties, İnterface state*

Submission Date: 30 August 2021
Acceptance Date: 29 October 2021

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1. Introduction

Metal–semiconductor (MS) electronic devices have great importance in the electronic applications. MS structures are frequently used in integrated circuits, in light detectors and solar cells in the electronic industry [1-4]. Metal-semiconductor (MS) photodiodes with graphene oxide (GO) and perylenetetracarboxylic dianhydride (PTCDA) interfacial layers have received a lot of attention recently as they are used in many different applications, especially optoelectronics. Because this GO and PTCDA interfacial layer plays a critical role in controlling current flow between MS [5-7], and this situation is also important to control the breakdown voltage and reduce leakage currents [5,8]. Thus, metal-semiconductor (MS) interfaces are an essential part of virtually all semiconductor electronic and optoelectronic devices.

In this study, our aim is to investigate experimentally investigate the electrical characteristics such as ideality factors (n), barrier heights (Φ_{bo}), series resistances (R_S), and reverse-saturation currents obtained from the forward bias I-V characteristics of the Al/GO-PTCDA/p-Si structures at absolute temperature (300 K).

2. Experimental details

In this study, we purchased PTCDA and GO organic semiconductor powder from Fytronix, but chemical solvents for cleaning substrates from Sigma-Aldrich. The Si crystal used in the preparation of photodiodes has a thickness of 525 μm in the [100] direction and a resistive structure of 2-10 Ω-cm. Firstly, the wafer cleaned using the cleaning process to remove contaminants from the semiconductor surfaces. The wafer was dried using nitrogen gas (N_2) after the cleaning procedure. With a thermal evaporation apparatus, Al (99.999 percent) metal was evaporated at 10^6 Torr for ohmic contact. After that, the Si wafer was cut into small pieces. The semiconductor wafer front faces were coated PTCDA-GO (1:1) solutions with spin speed of 1000 rpm for 30 s by spin coating method (6800 Spin Coater Series). Following these procedures, to make a rectifier Al metal contact with diameter of 1 mm at 10^6 Torr pressure Al (% 99.999) metal was thermally evaporated on the surface of organic layer-semiconductor pieces. The rectifier contact's area of the photodiode was found to be $3.14x10^{-2}$ cm^2. As conclusion, the cross-section of the Al/ PTCDA-GO/p-type Si/Al semiconductor structure is shown in Fig. 1. The temperature dependent IV measurements were performed by using a Keithley 2400 Source-Meter with the help of a Computer through an IEEE- 488 AC/DC converter card.

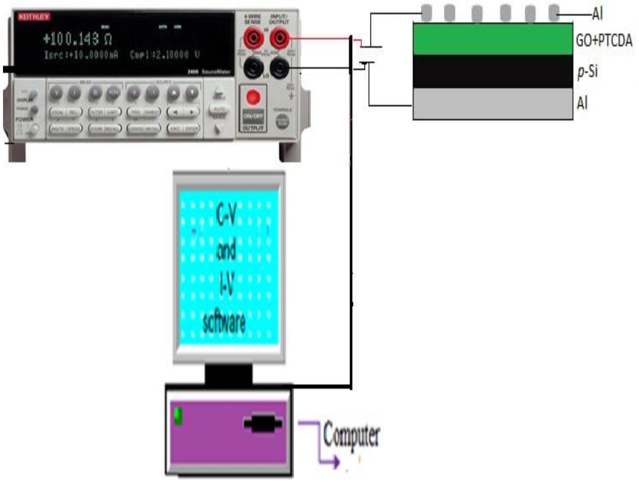

Fig.1. Schematic representation of the Al/GO-PCDA/p-Si structure and *I-V* measurement system

3. Results and discussion

The electrical characteristics Al/GO-PCDA/p-Si structures were monitored as a function of forward and reverse bias conditions at room temperature (300 K) and illustrated in Fig.2. As can be shown in the Fig. 1, for the both structures, the current curves increases exponentially with applied forward bias voltage.

From the thermionic emission (TE) theory, the experimental current-voltage characteristics are analyzed by following equation [1-8];

$$I = I_o \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

where q is the electron charge, V is applied voltage, *n* is the ideality factor, k is the Boltzman constant 1.38x10-23 $J\,K^{-1}$, *T* is the absolute temperature and I_o is the saturation current derived from the straight line intercept of lnI at *V*=0 and is given by;

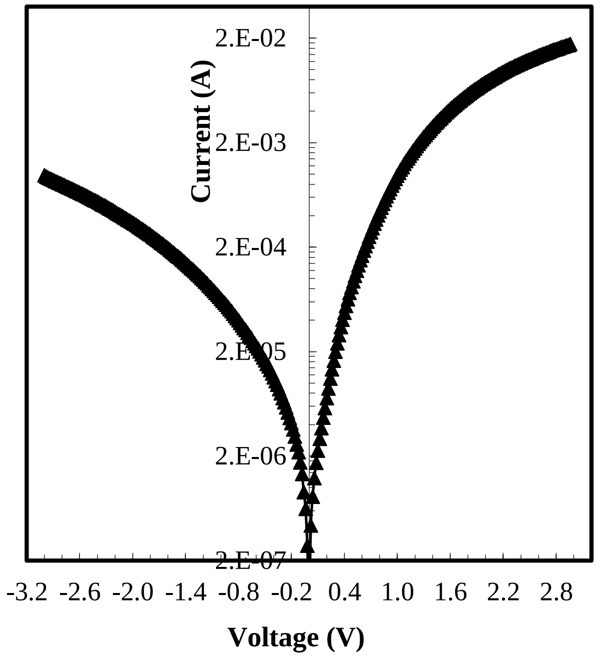

Fig. 2. The current–voltage plots of the Al/GO-PCDA/p-Si structure at room temperature

$$I_o = AA^*T^2\exp\left(-\frac{q\Phi_{bo}}{kT}\right) \quad (2)$$

where *A* is the effective diode area, *A** is the effective Richardson constant of 32 $Acm^{-2}K^{-2}$ for *p*-type Si, respectively. The ideality factor (*n*) of the Al/GO-PCDA/*p*-Si structure are determined from the slope of the linear region of the forward bias *I-V* measurements through the relation;

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln I}\right) \quad (3)$$

the barrier height (Φ_{bo}) is determined from the saturation current (I_o) and is given by the relation;

$$\Phi_{bo} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_o}\right) \quad (4)$$

Using Eq. (3) and Eq. (4) the values of the *n*, and Φ_{bo} of the Al/GO-PCDA/*p*-Si structure at room temperatures were calculated from the slopes of the linear region of the forward bias ln(*I*)-*V* plots in Fig. 2. The values 4.43 and 0.609 eV for the *n* and Φ_{bo} of the Al/GO-PCDA/*p*-Si structure, respectively. The ideality factor's value in this analysis is higher than unity (n = 1). This situation can be attributed to the fact that the PTCDA organic interlayer increased the effective barrier height by influencing the space charge region of Si.

Another method to determine the main parameters of metal-semiconductor structures is Cheung method [9]. According to Cheung function is analyzed by following equation;

$$\frac{dV}{d(lnI)} = n\frac{kT}{q} + R_S I \qquad (5)$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) = IR_S + n\Phi_{bo} \qquad (6)$$

Experimental *dV/d(ln I)* vs I and *H(I)* vs *I* plots of the of Al/GO-PCDA/*p*-Si structure at room temperature are presented in Fig.3, respectively. The slope and intercept of dV/dln(I)-I plots according to Eq. 5 would yield R_S and nkT/q, respectively. The values of idealitry factor and series resistance were found as 8.16 and 80.137 Ω for the Al/GO-PCDA/*p*-Si structure, respectively. At the same time, the slope and intercept of *H(I)-I* plots according to Eq. 6 would yield Rs and $n\Phi_{bo}$, respectively. The values of Φ_{bo} and R_S were found as 0.553 eV and 81.378 Ω for the Al/GO-PCDA/*p*-Si structure, respectively. This is that series resistance values obtained from Cheung functions are in good agreement with each other.

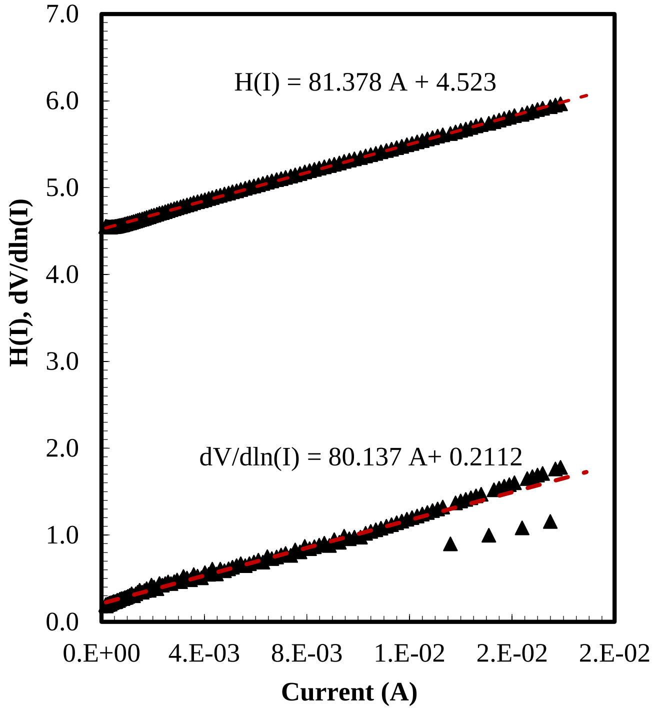

Fig. 3. *dV/d(ln I)* vs I and *H(I)* vs *I* plots of the of Al/GO-PCDA/*p*-Si structure

As you can see in Fig.3, these ideality factor values are higher than the values obtained from *I–V* curve. This situation can be attributed to the existence of the series resistance and the interface states. Also, the differences at the main electrical properties can be attributed to the approximation differences between the thermionic emission theory and Cheung methods.

Furthermore, Norde [10] suggested a method to determine the value of the series resistance in order to check the effect of series resistance on I–V curves. According to Norde's [10] functions Φ_{bo} and R_S are defined as in the following equations;

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \qquad (7)$$

$$\Phi_b = F(V_0) + \frac{V_o}{\gamma} - \frac{kT}{q} \qquad (8)$$

$$R_S = \frac{\gamma - n}{I_0}\ \frac{kT}{q} \qquad (9)$$

where γ is an constant higher than the ideality factor, $F(V_0)$ is the minimum point of *F(V)* vs *V* plot, V_0 and *I* are the corresponding bias voltage and current values, respectively. *F(V)- V* curves of the Al/GO-PCDA/*p*-Si structure at room temperature is shown in Fig. 4.

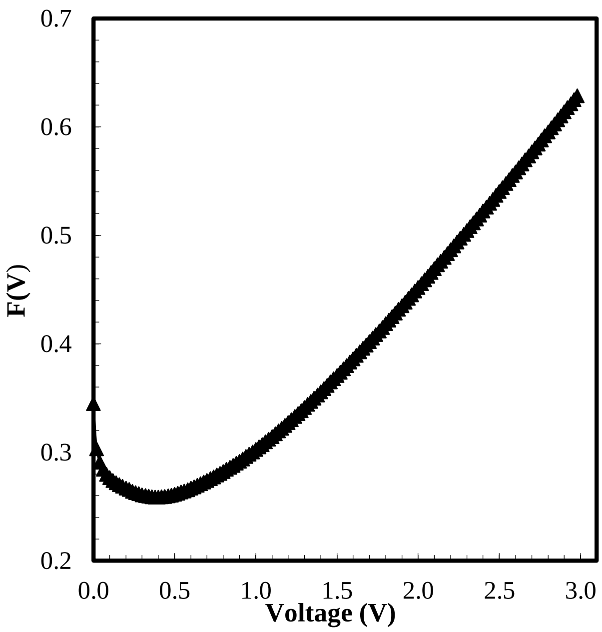

Fig. 4. The F(V)-V plots of Al/GO-PCDA/p-Si structure at room temperature

In Fig.4, the values of Φ_{bo} and R_S were obtained using Eq. (8) and Eq. (9). Thus, values of Φ_{bo} and R_S were found as 0.264 eV and 317.49 Ω for Al/GO-PCDA/p-Si structure, respectively. As can be seen, the barrier height values obtained from the Norde method are lower than the values obtained from the Cheung method. However, the values of series resistance obtained from Norde functions are higher than Cheung's functions. These differences may be attributed to the extraction from different regions of the forward-bias current–voltage plot. That is, this situation clearly shows that Norde's method are applied to the all forward bias regions of the *I–V* curve, while Cheung functions are only extended to the nonlinear region of the forward bias I–V curve.

At the same time, the interface states (N_{SS}) is a very another important parameter that effects on the basic parameters obtained from I–V measurements. Fig. 5 shows the interface state energy distribution curve of the Al/GO-PCDA/p-Si structure at room temperature. According to Card-Rhoderick [11] the N_{SS} densities can be written as follows:

$$qN_{SS}(V)=\left[\frac{\varepsilon_i}{\delta}(n(V)-1)-(\frac{\varepsilon_s}{W_D})\right] \qquad (10)$$

where W_D is the depletion-layer width, $n(V)$ is the voltage dependent of n ($n(V)=V/(kT/q)\ln(I/I_0)$), ε_s and ε_i are the dielectric of the semiconductor and interlayer, and δ is the interfacial-layer thickness, respectively.

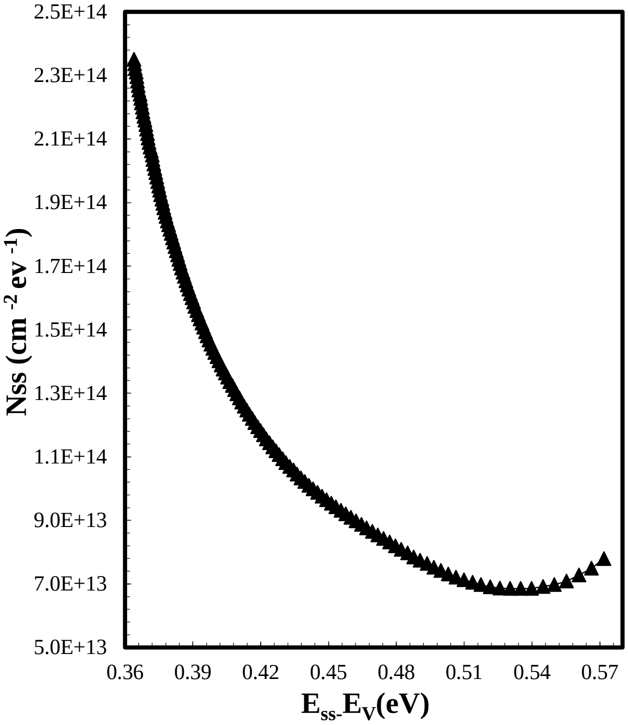

Fig. 5. The N_{SS}- (E_{SS}-E_V) plots of Al/GO-PCDA/p-Si structure at room temperature

Also, the energy distributions (E_{SS}-E_V) can be written as below;

$$E_{SS}-E_V=q\Phi_e-qV \qquad (11)$$

As can be Fig. 4, the interface state density (N_{SS}) calculated without taking into account series resistance (R_S) has increased exponentially with bias from 7.79x10^{13} cm^{-2}eV^{-1} in (0.572- E_V) eV to 2.31^{14} cm^{-2}eV^{-1} in (0.365- E_V) eV of p-Si. This case may be ascribed to the chemical reactivity of Schottky metal. Also, it is clear that the existence of GO and PTCDA interfacial layer improves the performance of MS structure.

4. Conclusions

In this work, we investigated the main electrical properties such as ideality factor (n), barrier height (Φ_{bo}) and series resistance (R_S) of the Al/GO-PCDA/p-Si structure using the current–voltage (I-V) characteristics at room temperature. The barrier height and series resistance values obtained from Cheung's method is lower than the one obtained from Norde method. This difference situations clearly shows that Norde's functions are applied to the all forward bias regions of the I–V plot of the structures, while Cheung functions are only extended to the nonlinear region of the forward bias I–V plot. Also, the interface states in equilibrium with the semiconductor were calculated from the downward curvature region caused by the presence of series resistance and interface states in the current–voltage plots.

Acknowledgement:

*This work was supported by Kahramanmaras Sütçü Imam University Scientific Research Project Unit (**Project numbers: 2020/9-30 D)**. We would like to thank Kahramanmaraş Sütcü Imam University for financial support of the research program*

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